

Figure 1

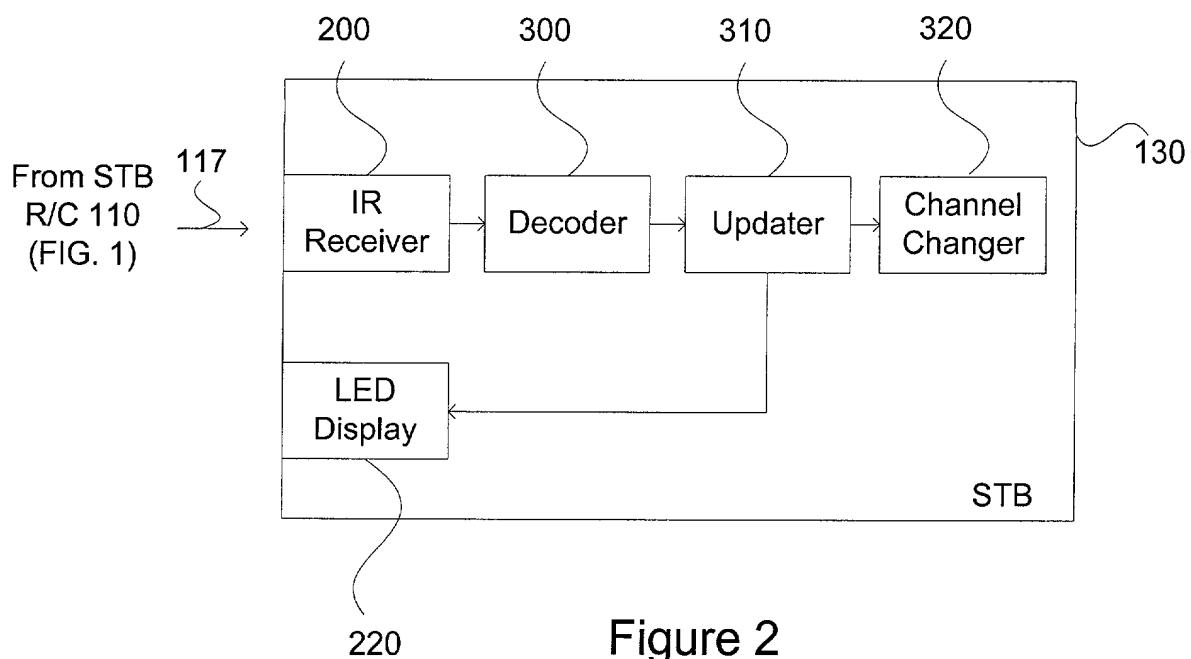


Figure 2

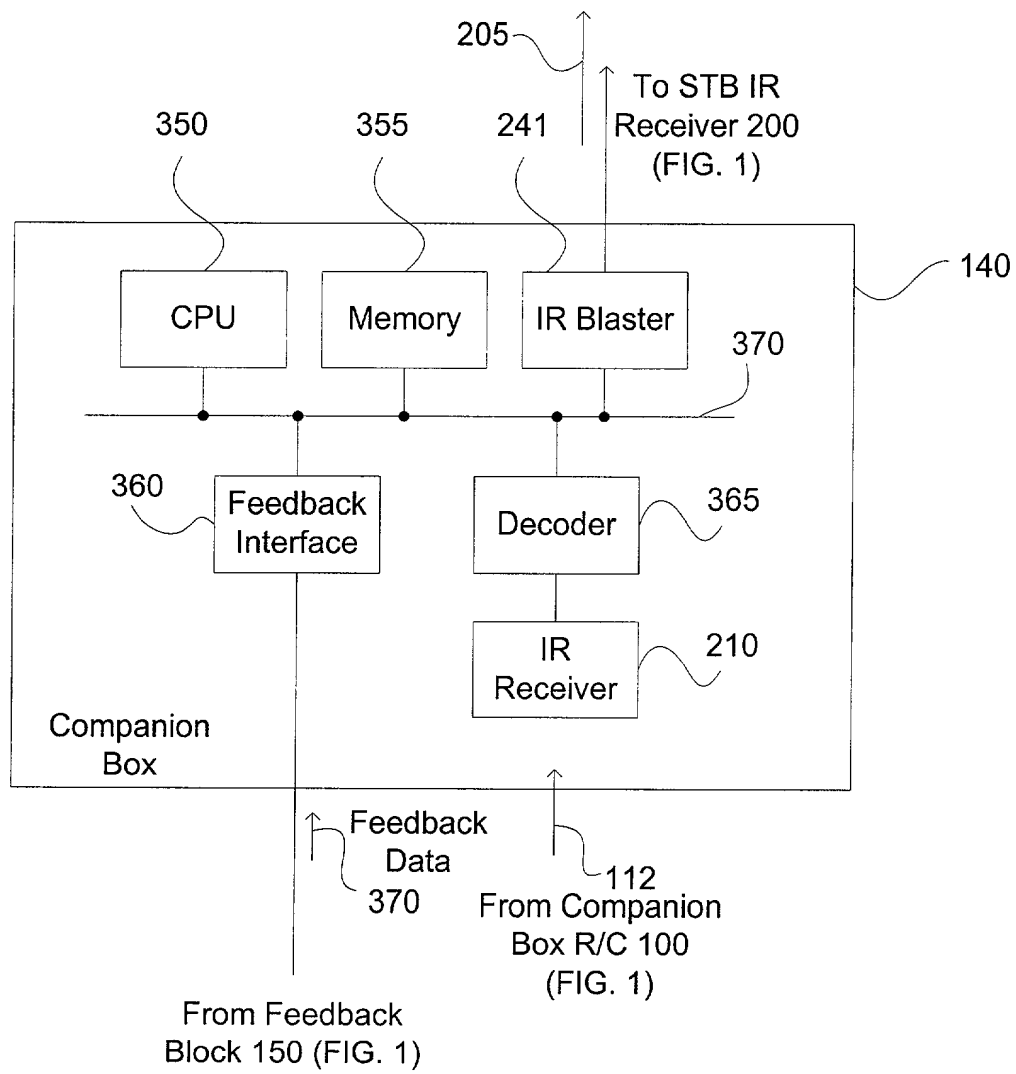


Figure 3

205

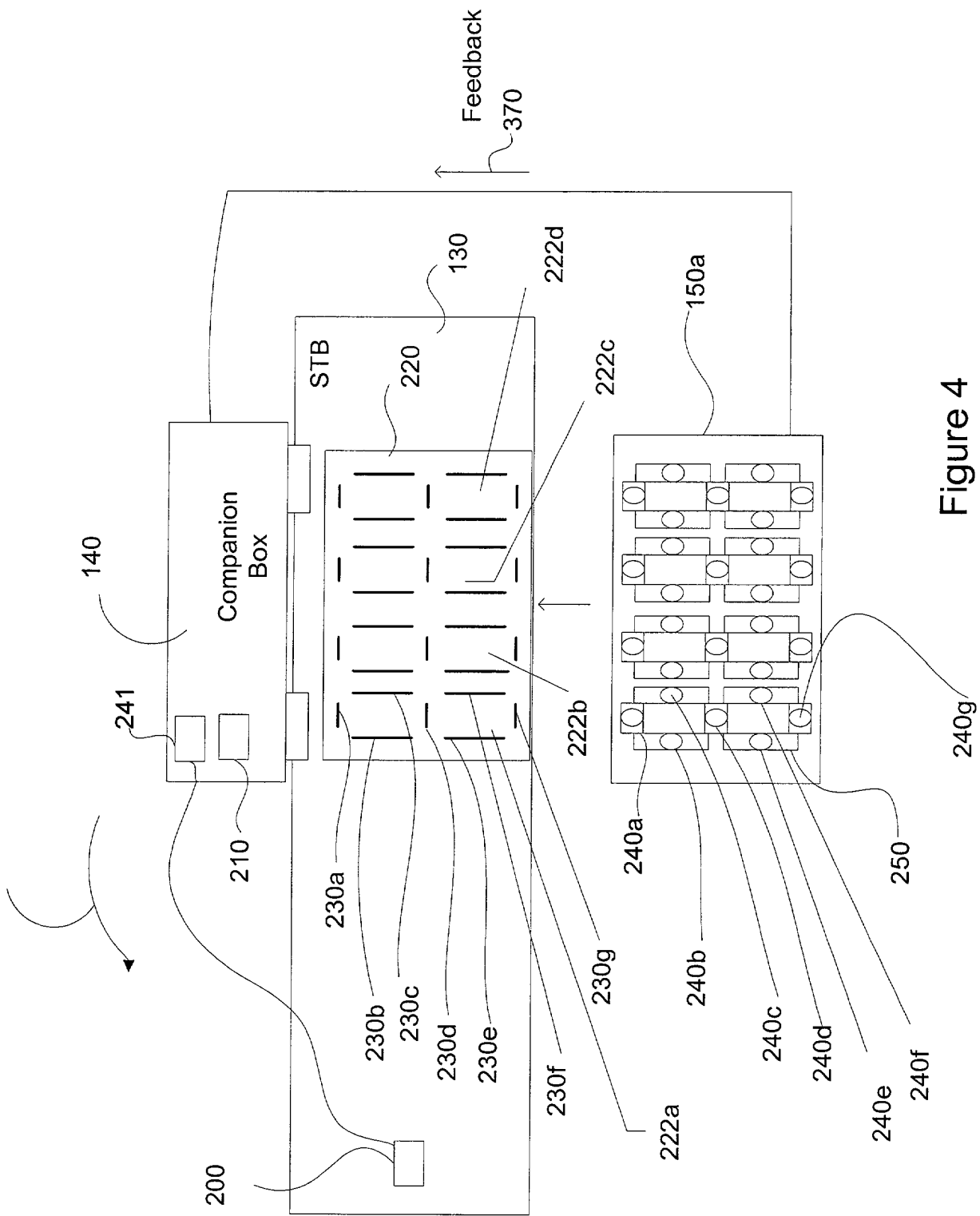


Figure 4

FIG. 5 is a block diagram of a system 100 in accordance with one embodiment of the present invention. The system 100 includes a sensor array 110, a multiplexer 120, a digital state machine 130, a threshold comparator 140, and a feedback interface 150.

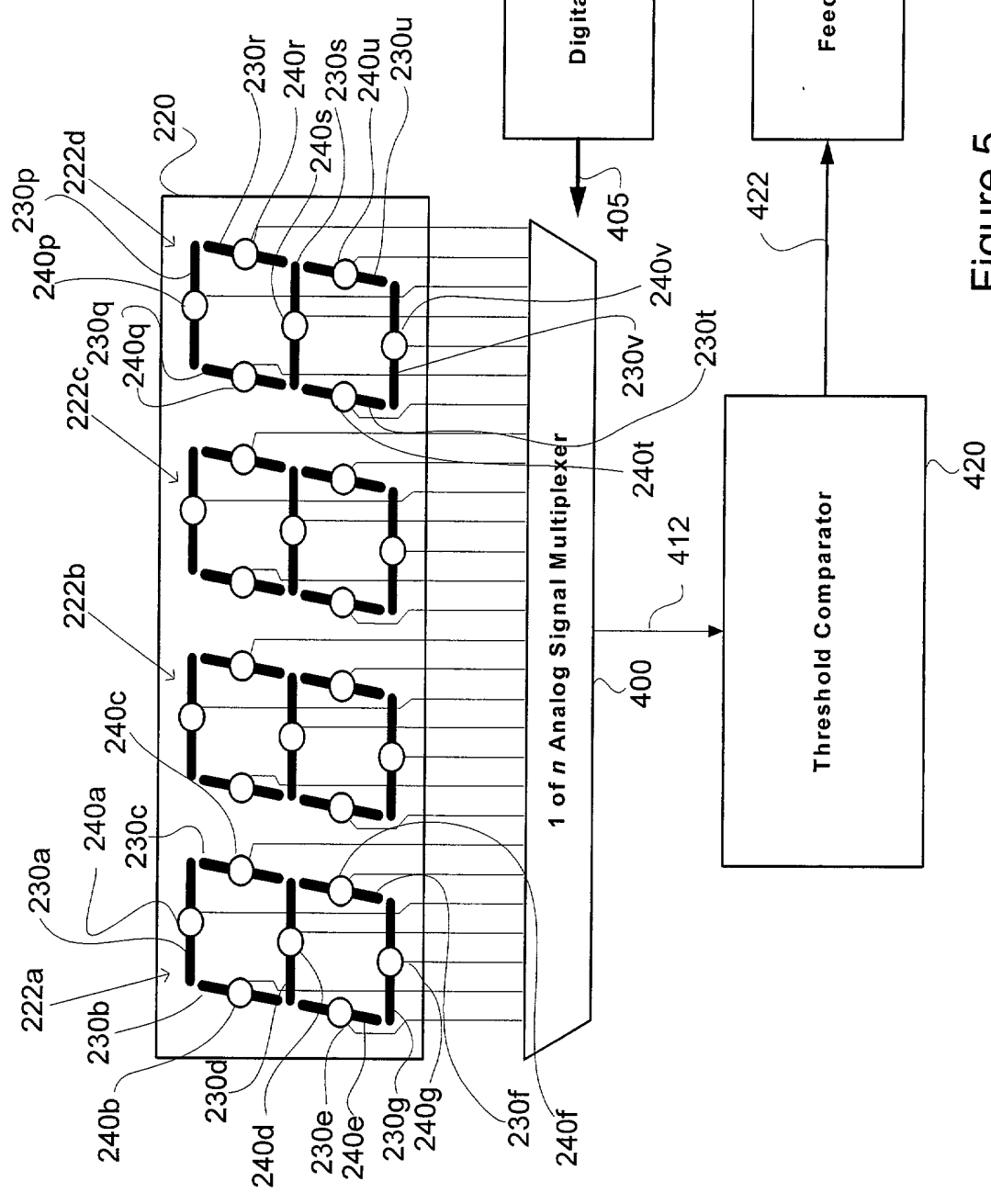


Figure 5

550

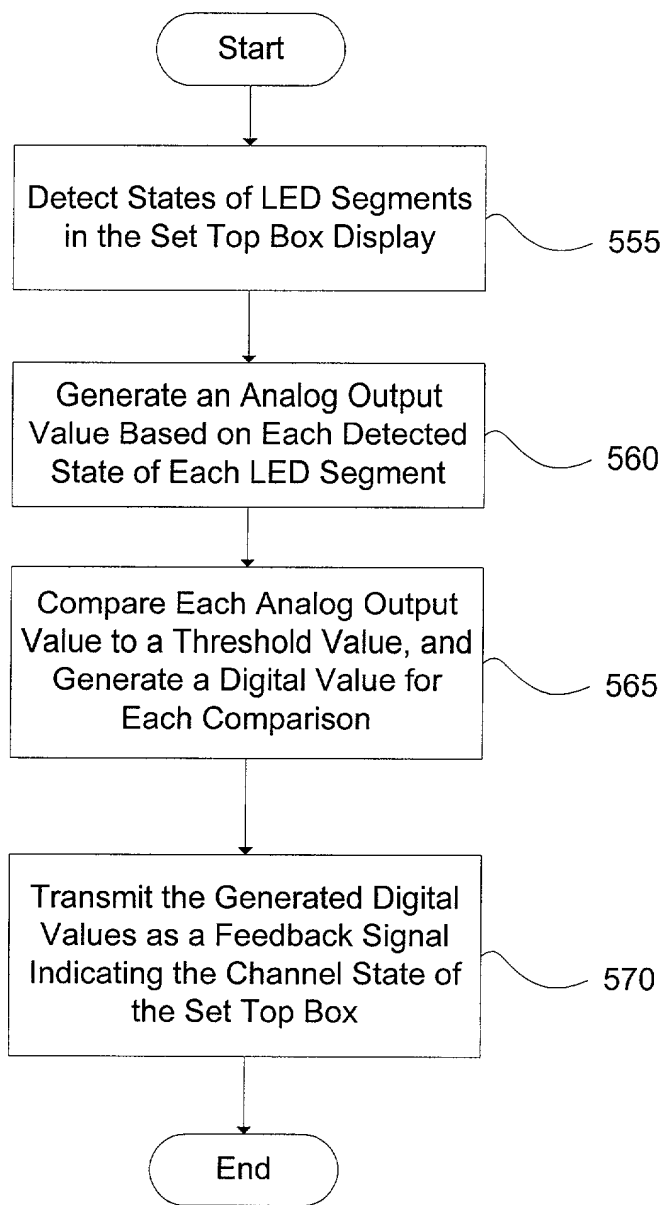


Figure 6

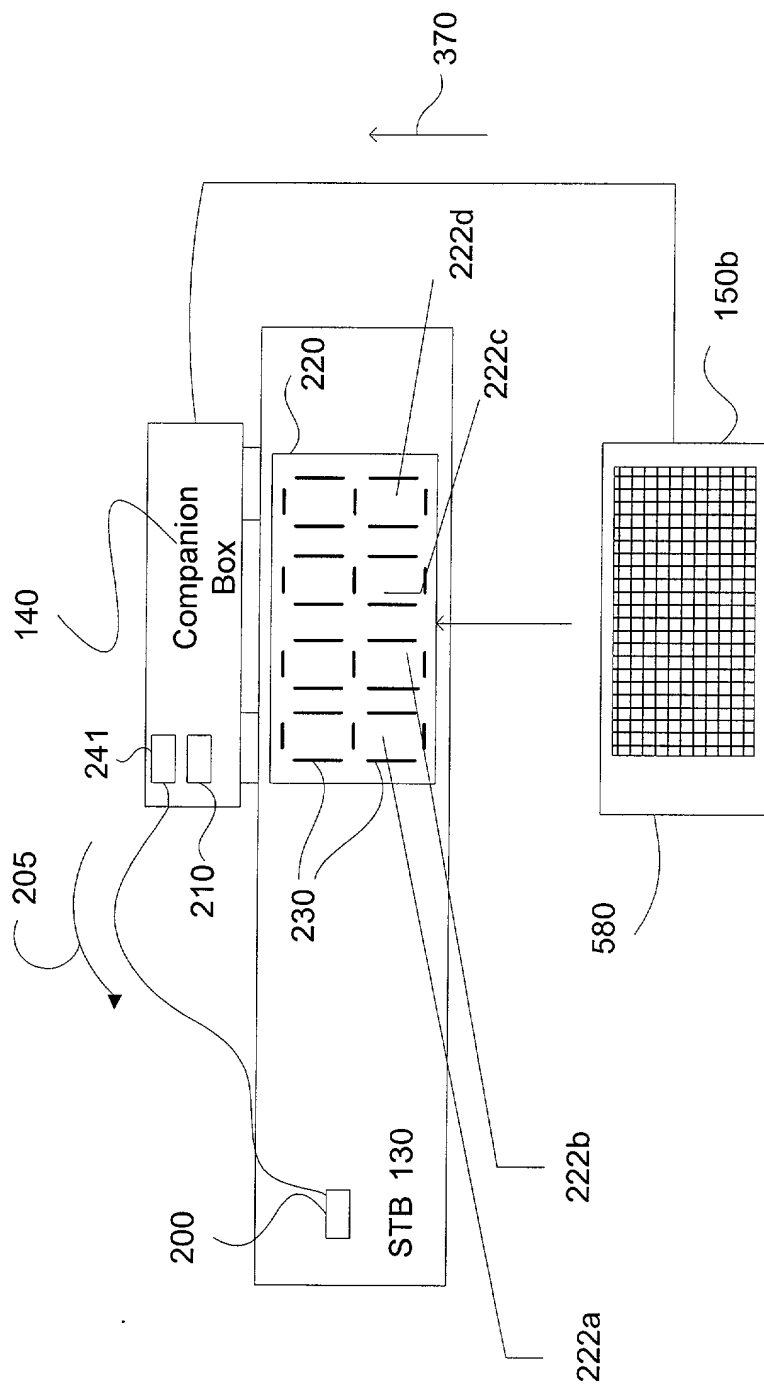


Figure 7

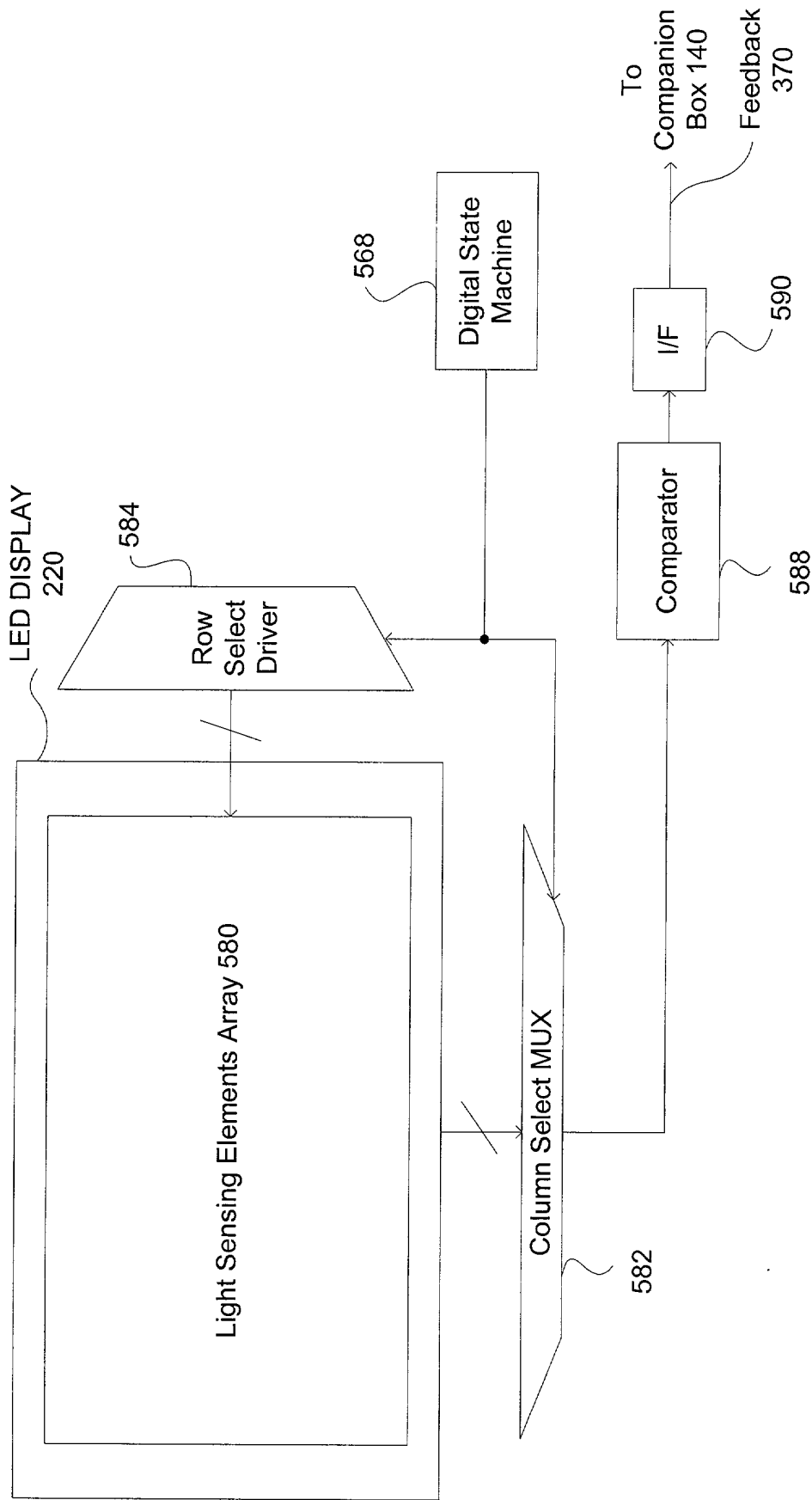


Figure 8



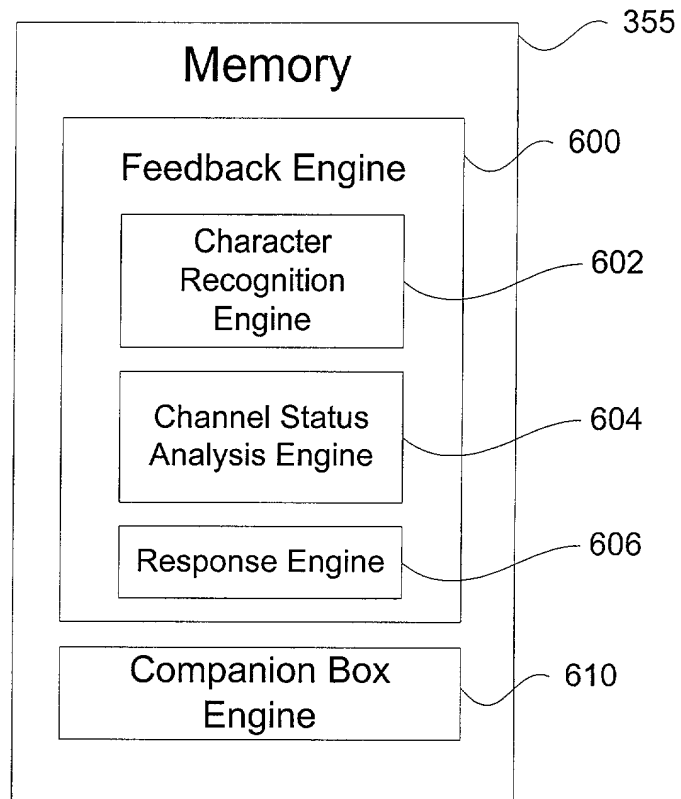


Figure 9

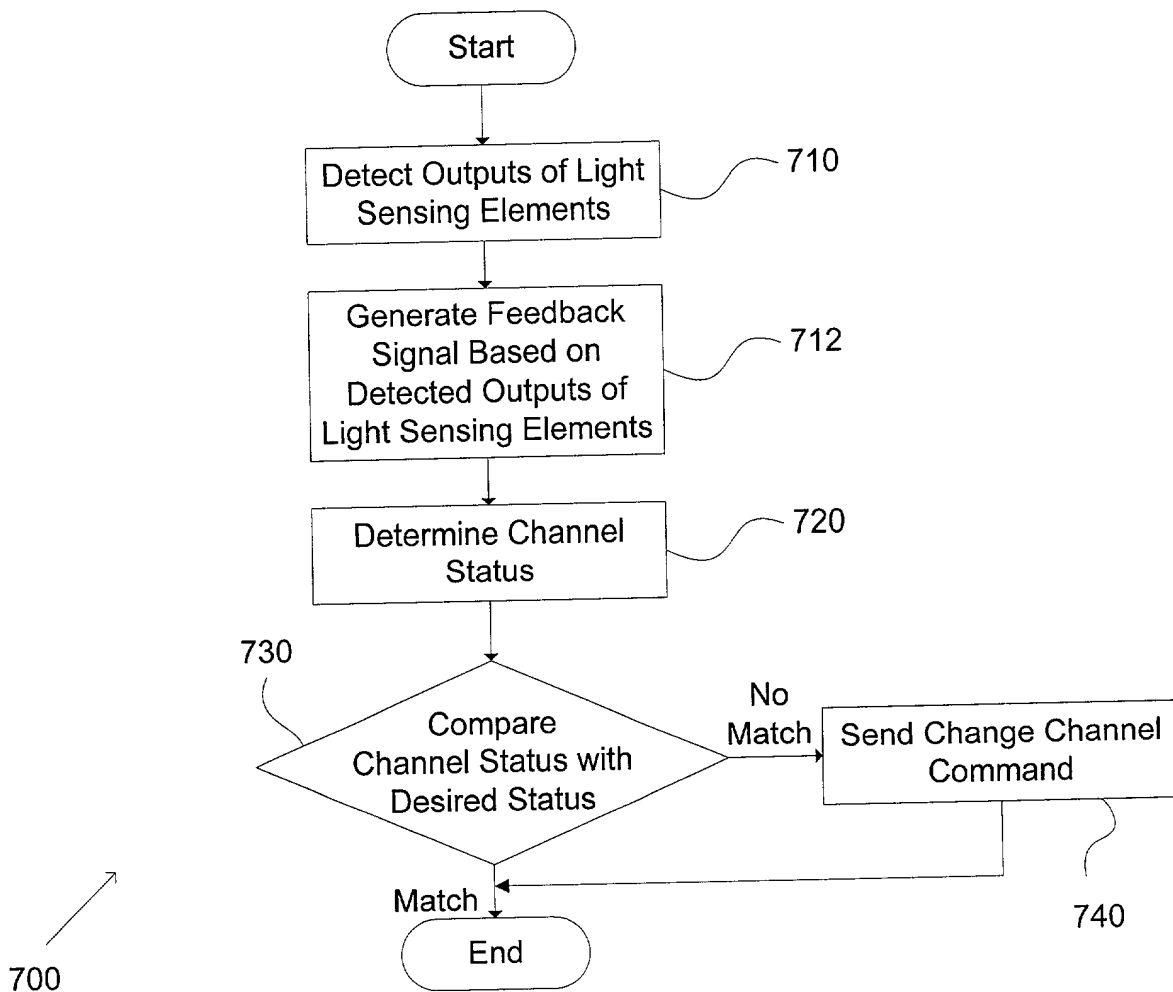


Figure 10